CLAIMS

1. A signal conditioning system, comprising:

a first converter;

a random clock, said random clock configured to decorrelate an input signal provided to said first converter from said random clock so that the average output signal of said first converter is proportional to a first offset signal; and

a first offset sensor connected to sense the first offset signal, and in response to said sensing, to condition said first converter output.

2. The system of claim 1 wherein, said random clock includes at least one of a random clock generator, a pseudorandom clock generator, and an aperiodic clock generator.

3. The system of claim 1 wherein, said random clock is configured to randomly select said first converter and to randomly sample the input signal to said first converter, at least one of the random sampling and the random selecting providing the average output of said first converter proportional to the first offset signal.

4. The system of claim 1 wherein, the first offset signal is subtracted from at least one of a first input and first output of said first converter.

5. The system of claim 1 wherein, said first offset sensor provides one of a feedback loop and a feedforward loop.

6. The system of claim 1, further including:

a second converter, said random clock being configured to decorrelate the input signal to said second converter from said random clock so that the average output signal of said second converter is proportional to a second offset signals;

a second offset sensor connected to sense the second offset signal, and in response to said sensing, to condition said second converter output.

7. The system of claim 6, further including a corrector coupled between said first and second converters, said corrector being configured to adjust the difference between the first and second offset signals.

8. The system of claim 6, further including a corrector coupled between said first and second converters, said corrector being configured to sense an offset mismatch signal between said first and second converters, the offset mismatch signal being proportional to the difference between the first and second offset signals.

9. The system of claim 6, wherein said first and second converters are selected in a random sequence correlated to a random sampling rate corresponding to said random clock.

10. An integrated circuit that converts between an analog signal and a corresponding digital code with a system sampling rate f_s, said circuit comprising:

a plurality of converter circuits clocked by a random clock, at least one converter circuit in said plurality of converter circuits sampling the analog signal at least every $1/f_s$ seconds; and

an offset sensing circuit configured to sense signal offsets and/or signal offset differentials between the outputs of said plurality of converter circuits.

11. The circuit of claim 10, wherein said offset sensing circuit includes a plurality of offset sensing sub-circuits, each offset sensing sub-circuit in said plurality of sub-circuits being configured to adjust the signal offset differential and/or signal offsets between respective pairs of converter circuits.

12. The circuit of claim 10, wherein the sampling is provided by a sampling circuit clocked by said random clock to decorrelate the analog input signal from a random clock signal provided by said random clock.

13. The circuit of claim 10, further including a controller circuit configured to detect instances when available converter circuits in said plurality of converter circuits are available to process an upcoming one of said random samples.

14. The circuit of claim 10, wherein said plurality of converter circuits are interleaved.

15. The circuit of claim 10, wherein said offset signal is subtracted from one of said input signal through a

feedback loop circuit and said corresponding output signal through a feedforward loop circuit.

16. The circuit of claim 10, wherein each offset sensing circuit includes at least one of a filter and an amplifier.

17. The circuit of claim 10, wherein each converter circuit in said plurality of converter circuits is corrected to one of a zero offset and another desired offset value.

18. The circuit of claim 10, wherein each converter circuit in said plurality of converter circuits is corrected to said offset signal of one converter circuit in said plurality of converter circuits.

19. A method of adjusting an offset signal in a signal conditioning system, comprising:

clocking a first converter with a random clock;

sensing a first offset signal of said first converter; and

conditioning one of an input signal and an output signal of said first converter with said first offset signal.

20. The method of claim 19, further including a step of sensing a second offset signal of a second converter, said second converter being clocked with said random clock.

21. The method of claim 20, further including a step of sensing a difference between said first and second offset signals.

22. The method of claim 21, further including a step of adjusting said difference between said first and second offset signals.

23. The method of claim 20, further including a step of sampling an input signal to said first and second converters with said random clock.

24. The method of claim 23, further including a step of selecting said first and second converters in a random sequence correlated to said random clock.

25. A signal conditioning system, comprising:

a first converter with a first gain and a second converter with a second gain, said first and second converters being clocked in a random sequence; and

a gain corrector configured to adjust a difference between said first and second gains.

26. The system of claim 25, further including at least one of a random clock generator, a pseudorandom clock generator, and an aperiodic clock generator to provide said random sequence.

27. The system of claim 25, wherein said gain corrector provides a difference between said first and second gains.

28. The system of claim 27, wherein said difference provides a gain correction signal to adjust said gain difference between said first and second converters.

29. The system of claim 25, wherein said gain corrector provides a gain correction signal proportional to a ratio between said first and second gains.

30. The system of claim 25, wherein said gain sensor forms one of a feedback loop and a feedforward loop.

31. The system of claim 25, wherein said gain sensor includes at least one of a filter and a rectifier.

32. An integrated circuit that converts between an analog signal and a corresponding digital code at a clock rate f_s, said circuit comprising:

a plurality of converter circuits clocked by a random clock;

a gain sensor circuit coupled to each converter circuit in said plurality of converter circuits, said gain sensor circuit sensing a gain from said corresponding converter circuit, each gain sensor circuit being coupled to one of said plurality of converter circuits; and

a controller circuit configured to select said plurality of converter circuits in a random sequence.

33. The circuit of claim 32, further including at least one sampling circuit that provides random samples of an input signal in successive $1/f_s$ clock periods, said at least one sampling circuit being clocked with a random clock signal from said random clock to decorrelate said input signal from said random clock signal.

34. The circuit of claim 33, wherein said controller circuit is further configured to detect instances when available converter circuits in said plurality of converter circuits are available to process an upcoming one of said random samples.

35. The circuit of claim 32, wherein said plurality of converter circuits are interleaved.

36. The circuit of claim 32, wherein an input signal provided to said plurality of converter circuits includes a zero-offset signal.

37. The system of claim 32, wherein said gain sensor circuit provides a gain correction signal proportional to a difference between said gain of said corresponding converter circuit and a reference gain of one other corrector circuit.

38. The system of claim 32, wherein said gain sensor circuit provides a gain correction signal proportional to a ratio between a gain of said corresponding converter circuit and a reference gain of one other corrector circuit.

39. The system of claim 32, wherein said gain sensor circuit forms one of a feedback loop and a feedforward loop.

40. The system of claim 32, wherein said gain sensor circuit includes at least one of a filter circuit and a rectifier circuit.

41. A method of adjusting a gain mismatch in a signal conditioning system, comprising:

sensing a first gain of a first converter;

sensing a second gain of a second converter, said first and second converters being clocked with a random clock; and

adjusting at least one of said first and second gains to adjust said gain mismatch between said first and second converters.

42. The method of claim 41, wherein the step of adjusting at least one of said first and second gains includes a step of sensing a difference between said first and second gains.

43. The method of claim 41, wherein the step of adjusting at least one of said first and second gains includes a step of sensing a ratio between said first and second gains.